UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,999	02/02/2004	Terunao Hanaoka	109690.02	5935

25944 7590 11/28/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
CAO, PHAT X	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,999	HANAOKA ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) *3 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/870,710.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/04 & 9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election of Group I (claims 1-2 and 5) in the reply filed on 9/12/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

2. Claims 2 and 5 are objected to because of the following informalities:

- in claim 2, line 2, "," should be inserted between "devices" and "adjacent".
- In claim 2, line 3, "the conductive layer" should be changed to "a conductive layer".
- In claim 2, line 7, "a conductive layer" should be changed to " said conductive layer".
- In claim 5, line 2, "an undermost semiconductor device" should be changed to "said undermost semiconductor device".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Imaoka et al (US. 5,825,080).

Regarding claim 1, Imaoka (Fig. 6) discloses a stack-type semiconductor device formed by stacking a plurality of semiconductor devices (11-1) – (11-4), at least an undermost semiconductor device (11-1) among the plurality of semiconductor devices, comprising: a semiconductor element 14-1 (column 1, lines 30-35) having a through hole and a plurality of electrodes (15-1) and (15-2) formed on a first surface of the semiconductor element; a conductive layer (20-11)/(20-12) which is electrically connected to the electrodes (15-11)/(15-12), and is provided from the first surface through an inner wall of the through hole to a second surface of the semiconductor element 14-1 which is opposite to the first surface; and a plurality of connecting portions (17-11)/(17-12) provided on the conductive layer (20-11)/(20-12) so that a distance between two connecting portions (17-11)/(17-12) among the plurality of connecting portions is different from a distance between at least two electrodes (15-11)/(15-12) among the plurality of electrodes on at least one of the first and second surfaces.

Regarding claim 5, Imaoka's Fig. 6 further discloses that the undermost semiconductor device (11-1) is arranged so that the first surface (16-1) of the semiconductor element 14-1 faces other stacked semiconductor device.

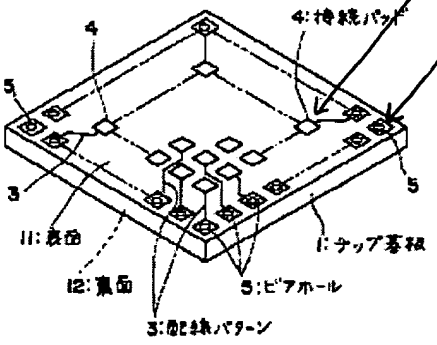
5. Claims 1-2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 05-029537 – cited by Applicant.

Regarding claims 1-2, JP ('537) (Figs. 1-3) discloses a stack-type semiconductor device formed by stacking a plurality of the semiconductor devices 1, adjacent semiconductor devices 1 among the plurality of the semiconductor devices being electrically connected by a conductive layer 3, each semiconductor device 1 comprising:

a semiconductor element 13 (par. [0012]) having a through hole 5 and a plurality of electrodes (corresponding to ring metal pads surrounding the top surfaces of through holes 5 shown in Fig. 1) formed on a first surface of the semiconductor element 13; the conductive layer (corresponding to the combination of the conductive layer formed inside the through hole 5 and the conductive layer 3) which is electrically connected to the electrodes, and is provided from the first surface through an inner wall of the through hole 5 to a second surface of the semiconductor element 13 which is opposite to the first surface; and a plurality of connecting portions 4 provided on the portion of the conductive layer 3 (see Fig. 1) so that a distance between two connecting portions 4 among the plurality of connecting portions is different from a distance between at least two electrodes (corresponding to ring metal pads surrounding the top surfaces of the through holes 5) among the plurality of electrodes, on at least one of the first and second surfaces.

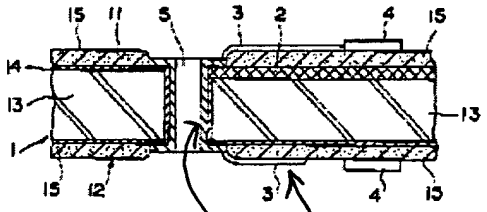
【図1】

本発明の実施例を示す説明図



【図2】

本発明の断面を示す説明図



【図4】

Regarding claim 5, JP ('537) further discloses that the undermost semiconductor device 1 (see Fig. 3) is arranged so that the first surface of the semiconductor element 13 faces other stacked semiconductor devices 1.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
November 22, 2005

PHAT X. CAO
PRIMARY EXAMINER